A METHOD AND APPARATUS FOR CONTROLLING POWER CONSUMPTION IN AN INTEGRATED CIRCUIT

DESCRIPTION

[Para 1] Field of the Present Invention

[Para 2] The present invention generally relates to devices used in integrated circuits for controlling power consumption, and more specifically, to devices that manage the power and information provided to components in the integrated circuit.

[Para 3] Description of Related Art

[Para 4] The advances in semiconductor and computer technology have resulted in computer systems becoming exponentially faster while occupying less physical space. The consumer space of desktop, lap-top, and PDA style computer systems are now operating at processing speeds that were once exclusively reserved for main frame systems. The appetite of the consumer for ever increased speed, functionality and decreased size has challenged the technology industry to overcome perplexing issues involving power and heat.

[Para 5] The speed of a particular device and the amount of power consumed during its operation are currently in a monotonic relationship (i.e. the faster the device, the more power required to operate the device). Mobile devices receive their power from batteries, and although various technological improvements have been made with respect to increasing the output and life of the battery itself, the mobile devices remain particularly sensitive to conserving power while maintaining speed and functionality. Although mobile

devices are the driving force for conserving power, non-mobile devices such as desktops have a vested interest as well.

[Para 6] It would, therefore, be a distinct advantage to have a method and apparatus for reducing the power consumption in an integrated circuit. The present invention provides such a method and apparatus.

[Para 7] SUMMARY OF THE PRESENT INVENTION

[Para 8] The present invention controls the power consumption in an integrated circuit by controlling the power level supplied to a particular unit and the tasks handled by the unit itself. More specifically, the present invention uses a complementary unit for a corresponding unit in the integrated circuit where power consumption control is desired. The complementary unit supports all or some of the tasks executed by the corresponding unit. The complementary unit is responsible for controlling which tasks are executed by the corresponding unit or itself according to a power management scheme. Depending upon the particular power management scheme used, the complementary unit can also control the power level of the corresponding unit for tasks that the corresponding unit handles.

[Para 9] BRIEF DESCRIPTION OF THE DRAWINGS

[Para 10] Figure 1is a block diagram illustrating one method used to eliminate power dissipation for an idle unit such as a processor;

[Para 11] Figure 2 is a timing diagram illustrating the performance and time required by a processor to complete a given task;

[Para 12] Figure 3 is a timing diagram illustrating the performance, time, and supply voltage required by a processor to complete the tasks shown in Figure 2;

[Para 13] Figure 4 is a schematic diagram illustrating a system in which a PPMU dynamically controls the powering-up and powering-down of a

processor according to the teachings of a preferred embodiment of the present invention.

[Para 14] Figure 5 is a flow chart illustrating the method used by the PPMU 414 for controlling the power consumption of the Processor 402 of the system of Figure 4 according to the teachings of the present invention.

[Para 15] DESCRIPTION OF THE PREFERRED EMBODIMENT

[Para 16] The present invention controls the power consumption in an integrated circuit by controlling the power level supplied to a particular unit and the tasks handled by the unit itself. More specifically, the present invention uses a complementary unit for a corresponding unit in the integrated circuit where power consumption control is desired. The complementary unit supports all or some of the tasks executed by the corresponding unit. The complementary unit is responsible for controlling which tasks are executed by the corresponding unit or itself according to a power management scheme. Depending upon the particular power management scheme used, the complementary unit can also control the power level of the corresponding unit for tasks that the corresponding unit handles.

[Para 17] The present invention uses the term Programmable Power Management Unit (PPMU) to describe a preferred embodiment of the complementary unit. It should be realized, however, that the present invention is not intended to be limited to what has been traditionally referred to as a power management unit, but to any unit that is responsible for managing the powering-up, powering-down, intercepting and processing tasks that could be processed by corresponding unit(s) under its control according to a power management scheme.

[Para 18] The preferred embodiment of the present invention uses the PPMU in the context of controlling a processor. It should be noted, however, that this is only a single preferred application, and that the present invention is

equally applicable to other applications where the PPMU performs the functions described above.

[Para 19] Reference now being made to Figure 1, a block diagram is shown illustrating one method used to eliminate power dissipation for an idle unit such as a processor 100. The most effective way to eliminate power dissipation for a processor 100 or other idle unit is to turn off its power supply. Conceptually, this is a very simple operation. The operation includes inserting a switch on the power supply of the unit, and turning the switch on or off according to the power management control as noted by processor 102. The use of a switch guarantees the absolute minimum power consumption during shutdown periods.

[Para 20] The ideal switch depicted for processor 102 is a drastic simplification of reality. Any real switch has an associated resistance and delay. Processor 104 illustrates a more realistic model of how the power supply can be turned off. The effect of the switch resistance and of the control delay must be taken into account when evaluating the opportunity to power-off the processor 104.

[Para 21] Even the processor 104 is a drastic simplification of reality. In actual circuits, a stabilized voltage supply is required. The presence of a stabilization delay limits the applicability of power-managed solutions to resources that are idle for time intervals much longer than stabilization delay. Several other difficulties including transient noise generated by turning on and off the supply voltage are involved in the power supply shutdown scheme as explained in connection with Figure 2.

[Para 22] Reference now being made to Figure 2, a timing diagram is shown illustrating the performance and time required by a processor to complete a given task. Specifically, the x-axis represents time and the y-axis represents the required performance of the processor to complete the task (1-4). In this example, four tasks are illustrated each requiring differing times for completion and performance. The time during which the processor is idle after each completion of the execution of a particular task is also noted.

[Para 23] Reference now being made to Figure 3, a timing diagram is shown illustrating the performance, time, and supply voltage required by a processor to complete the tasks shown in Figure 2. Again, the x-axis represents time and the y-axis represents the required performance of the processor to complete the task (1-4). Figure 3 also shows the amount of supply voltage required to complete a given task, and if the processor is idle between tasks, how much time is required to establish a stabilized voltage supply when the voltage supply shut off scheme is used. It should be noted that for the exemplary tasks 1-4 the idle time of the processor is equivalent to the amount of time required to power-up the idle processor, and therefore, no power savings are realized.

[Para 24] In the preferred embodiment of the present invention, the PPMU has a constant supply voltage while it controls the powering-up and powering-down of the processor. In addition, the PPMU can further enhance power reduction by having the capability to process a subset of tasks supported by the processor. With this capability, the PPMU can optimize the power management policy for each task designated for execution by the processor. In accordance with the optimized power management policy for a given task, the PPMU dynamically decides whether the task should be assigned to the processor or handled by the PPMU itself as explained in greater detail in connection with Figure 4.

[Para 25] Referring now to Figure 4, a schematic diagram is shown illustrating a system 400 in which a PPMU 414 dynamically controls the powering-up and powering-down of a processor 402 according to the teachings of a preferred embodiment of the present invention. The system includes an interface chip 404, Universal Interrupt Controller (UIC) 410, Memory 406, Peripherals 408, Main Processor 402, Power Regulator/Controller 412, and PPMU 414.

[Para 26] The Interface Chip 404 provides an interface to Memory 406, and peripherals 408 which can be either external or internal to the integrated circuit.

[Para 27] The UIC 410 controls interrupt handling and access to the Main Processor 402. In this case, the UIC 410 provides requests for interrupts directly to the PPMU to determine how they are handled. The UIC 410 also provides all external interrupt requests (e.g. Memory 406) for access to the Main Processor 402 to the PPMU 414.

[Para 28] The Power Regulator/Controller 412 controls the power for the powering-up and powering-down of the Main Processor 402 upon receiving appropriate commands from the PPMU 414.

[Para 29] Main Processor 402 includes a core, caches and a Bus Interface Unit (BIU). The use of these components is well understood, and therefore, further explanation is deemed unnecessary. The Main Processor 402 may be, for example, a PowerPC 604 produced by International Business Machines.

[Para 30] PPMU 414 includes a core, BUI, and caches. Again, the use of these components is well understood, and therefore, further explanation is unnecessary, except with respect to their function in connection with the preferred embodiment of the present invention as explained below.

[Para 31] The PPMU 414 will provide some or all of tasks supported by the Main Processor 402 depending upon the particular power saving scheme used and the design/ instruction set used. The power saving scheme should be designed in such a manner so as to allow the Main Processor 402 to operate at a high level of performance during its activation, and not encumbered by the PPMU 414, and at the same time allow maximum power savings when the Main Processor 402 is inactive and only the PPMU 414 is active.

[Para 32] In the preferred embodiment of the present invention, the Main Processor 402 is in communication with the PPMU 414 via a chip-to-chip bus 418 such as I2C. In the preferred embodiment, the Main Processor 402 and PPMU 414 have their own internal memory caches, with capacities and organizations that are appropriate to the required power and performance demands. It should be noted that the PPMU 414 and Main Processor 402 could

be implemented on the same die and share caches and the chip-to-chip bus 418 would not be required in such an embodiment.

[Para 33] The PPMU 414 maintains control over the Processor 402 with the assistance of the Power Regulator/Controller 412, Interface Chip 404, and UIC 410. The PPMU 414 establishes the voltage level provided to power the Processor 402 via the Power Regulator/Controller 412 by providing a voltage reference level. All external interrupts are provided to the PPMU 414 via the UIC. The PPMU 414 can process the interrupt itself, if supported, or pass the interrupt to the Processor 402, waking the Processor 402 from an idle state, if necessary. The PPMU 414 can also control power management functions internal to the main processor. In example, the Processor 402 clock frequency is controlled by divider circuits in its Phase Locked Loop (PLL). The PPMU 414 can control the divider values to scale the Processor 402 frequency to dynamically match current processing requirements. In further example, if the Processor 402 supports the concept of having control over power supplied to individual components, then the PPMU 414 can also provide control over these individual components as well. The operation of the PPMU 414 in implementing a power control scheme for the Processor 402 is explained in greater detail in connection with Figure 5.

[Para 34] Figure 5 is a flow chart illustrating the method used by the PPMU 414 for controlling the power consumption of the Processor 402 of system 400 (Fig. 4) according to the teachings of the present invention. The PPMU 414 analyzes the properties of each task that is directed towards the Processor 402 to determine whether the task is supported by itself or requires higher performance than it can provide (Step 500). If the task is supported by the PPMU 414 and does not require a performance level that exceeds that which the PPMU 414 can provide (Step 502), then the PPMU 414 executes the task (Step 504). The PPMU 414 then continues to analyze tasks as previously stated (step 500).

[Para 35] If, however, the task is not supported by the PPMU 414 or requires a performance that exceeds that which the PPMU 414 is capable of

providing (Step 502), then the PPMU 414 powers-up the Processor 402 and passes the task for execution (Step 506). The powering-up of Processor 402 is accomplished by having the PPMU 414 execute a predetermined sequence. The sequence includes raising the power supplied to the Processor 402 to a level required for execution of the received task by providing a reference voltage to the Power Regulator/Controller 412. For example, if the header devices on the Processor 402 have been turned off to block certain internal portions, then the PPMU 402 activates these devices. Using a timing loop or detection circuit, the PPMU 414 waits for or monitors the voltage until it reaches its desired level (e.g. an interrupt from the Power Regulator/Controller 412).

[Para 36] The sequence includes setting the state of the Processor 402 to some minimal level to allow bootstrapping itself to an active state. This can be accomplished in several different ways. One such way, is saving most of the required state on the Operating System (OS) memory stack, and forcing an interrupt in the Processor 402 whose handler restores the Processor 402 state from the stack. The stack location itself can reside in a register that the PPMU 414 can access or some other known location.

[Para 37] The sequence continues with the PPMU 414 ungating the clocks to the Processor 402 which takes the interrupt, boots up its machine state, and begins executing the application code. It should be noted that while the Processor 402 is executing the task, the PPMU 414 suspends its own execution of the main thread, but can execute maintenance code, and continue to provide other services. For example, the PPMU 414 can snoop the bus to maintain the coherency of its caches.

[Para 38] After the task has been executed by the Processor 402 at the performance level set by the PPMU 414, the Processor 402 returns control to the PPMU 414 (Step 508). This is accomplished by the Processor 402 flushing its caches and disabling them so that the array voltage can be reduced to a retention level or turned off completely. Alternatively, by continuing to run the snoop logic on the cache tag arrays, the state of those caches could be

maintained. The Processor 402 continues by saving its state on the OS stack, and sets a bit in a register that signals the PPMU 414. The PPMU 414 gates the clocks to the Processor 402, and begins executing the main thread starting from a known address, such as an interrupt vector. The PPMU 414 restores its own state, and continues to analyze tasks as stated above (Step 500).

[Para 39] It is thus believed that the operation and construction of the present invention will be apparent from the description provided. While the method and apparatus shown and described has been characterized as being preferred, it will be readily apparent that various changes and/or modifications can be made wherein without departing from the spirit and scope of the present invention as defined in the claims.